A General Partition Scheme for Gate Leakage Current Suitable for MOSFET Compact Models

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Outline

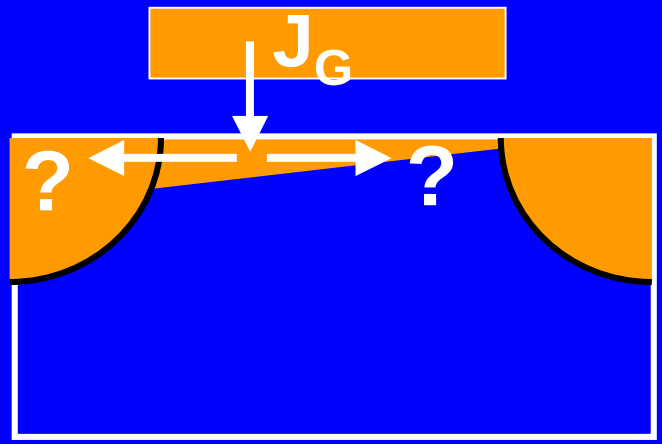
- Overview
- Model Derivation
- Numerical Validation
- Summary

Compact Modeling Needs

- Gate leakage poses a major challenge with aggressive T_{OX} scaling.
- Dropping V_{CC} demands higher accuracy for compact models.
- Both I_G and its source/drain partition are important.
- Accurate I_G correction needed to extract I_{DS} from measurement.

Problem Statement

- What is the general rule governing the source/drain partition of gate leakage current?



- Desire a partition scheme
  - valid for all bias conditions
  - independent of detailed model formulations
  - valid even in the presence of strong channel de-biasing

Existing Solutions

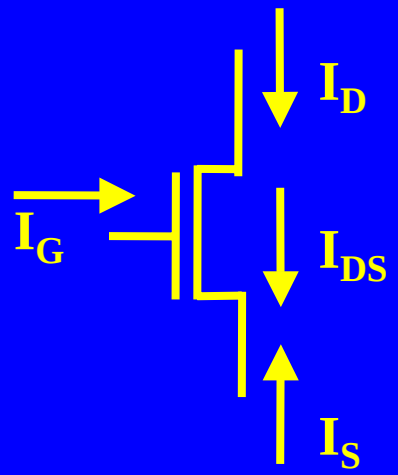
- **Lumped partition model[1]**
  - **J_G not distributed along channel.**
  - **I_{GS} independent of V_{DS}.**
- **Distributed partition model[2,3]**
  - **specific to the treatment of underlying J_G.**
  - **Valid in the weak tunneling regime where I_G effect on surface potential can be treated with perturbation.**
  - **Partition beyond the perturbation approximation not addressed.**

[1] Choi *et al.*, IEDM Tech. Dig. P.735, 1999.
[2] Cao *et al.*, IEDM Tech. Dig. p.815, 2000.
[3] Langevelde, Nat. Lab. Unclassified Report NL-UR2001/813, April 2001

Model Derivation

Definition of I_{GS} and I_{GD}

- (I_{DS}, I_{GS}, I_{GD}) cannot be uniquely determined from measured (I_D, I_S, I_G).
  - E.g. (0, $-I_S$, $-I_D$) is a possible solution.
- Values of I_{GS} and I_{GD} are only meaningful with respect to a given I_{DS}.
- Assigning the drain current *in the absence of* I_G to I_{DS} fixes I_{GS} and I_{GD}.



$$I_{GS} \equiv -I_S - I_{DS}$$

$$I_{GD} \equiv I_{DS} - I_D$$

Green's Function Approach

Transport equation:

$$\frac{\mu C_{ox}}{2\alpha}\frac{d^2U^2}{dy^2} = J_G$$

$$U \equiv V_{GS} - V_{TH} - \alpha(\varphi_s - \varphi_{ss})$$

J_G : Gate current density

μ : Mobility

φ_s : Surface potential

α : Body factor

$$U^2 = U_0^2 + U_1^2$$

U_0 : Homogeneous solution

U_1 : Correction due to J_G

$$U_1(y)^2 = \int_0^L G(y, y_0) J_G(y_0) dy_0$$

$$I_{GS} = \int_0^L (1 - y_0 / L) J_G(y_0) dy_0$$

Condition $U_1 << U_0$ is not needed

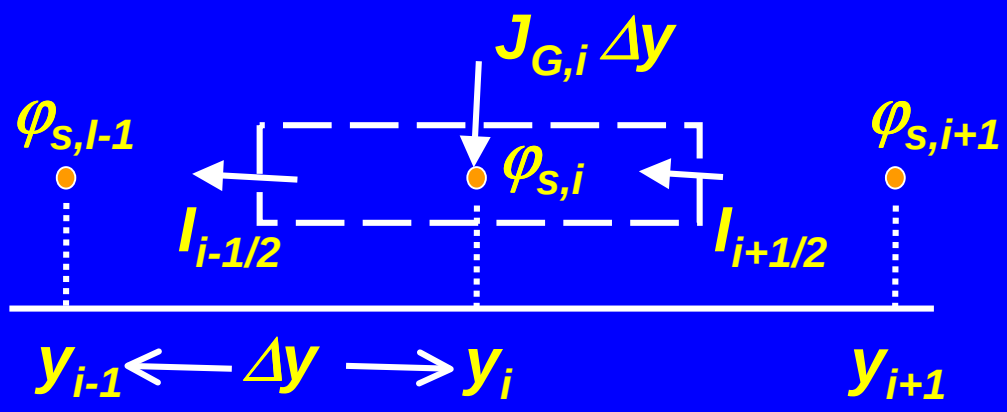
A General I_G Partition Scheme

- The source/drain partition for I_G is identical to that for inversion charge**.
- Applies to both weak and strong tunneling regimes.
- No assumption on specific functional form of J_G is necessary.
- Error due to constant-mobility assumption insignificant.

**D. Ward and R. Dutton, IEEE J. Solid-State Ckts., vol.SC-13, p.703, 1978.

Numerical Validation

Numerical Solution



$$I_{i+1/2} = \mu C_{ox} U_{i+1/2} \frac{\varphi_{s,i+1} - \varphi_{s,i}}{\Delta y}$$

$$I_{i+1/2} - I_{i-1/2} = -\Delta y J_{G,i}$$

- 1-D box integral.
- Fully consistent with underlying compact model.
- J_G model based on WKB approximation.
- Source-side φ_{ss} solved from 1-D Poisson equation.
- Drain-side $\varphi_{sd} = \varphi_{ss} + V_{dseff}$

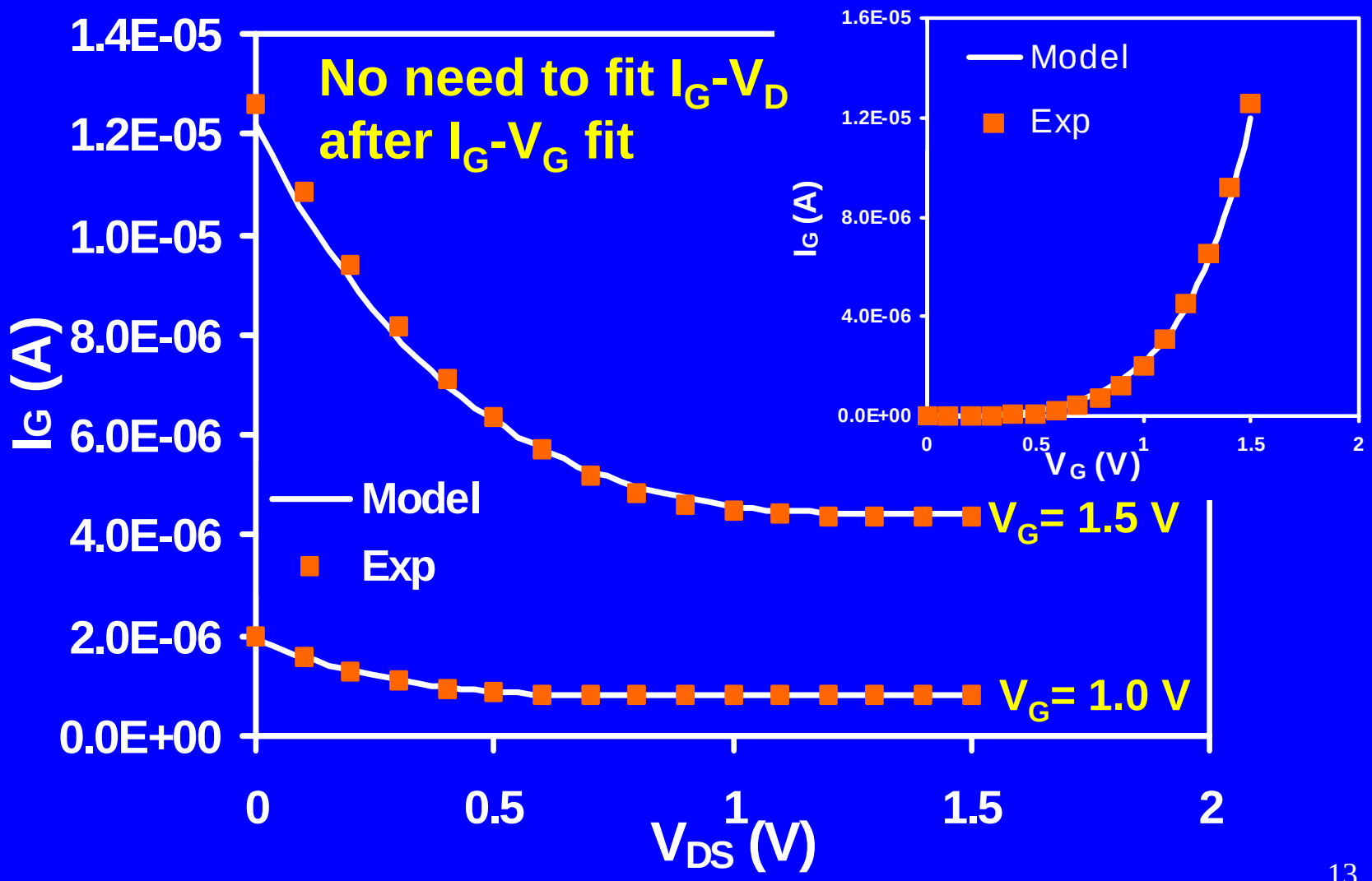
A hybrid model inside a SPICE-like circuit simulator

Model Parameters

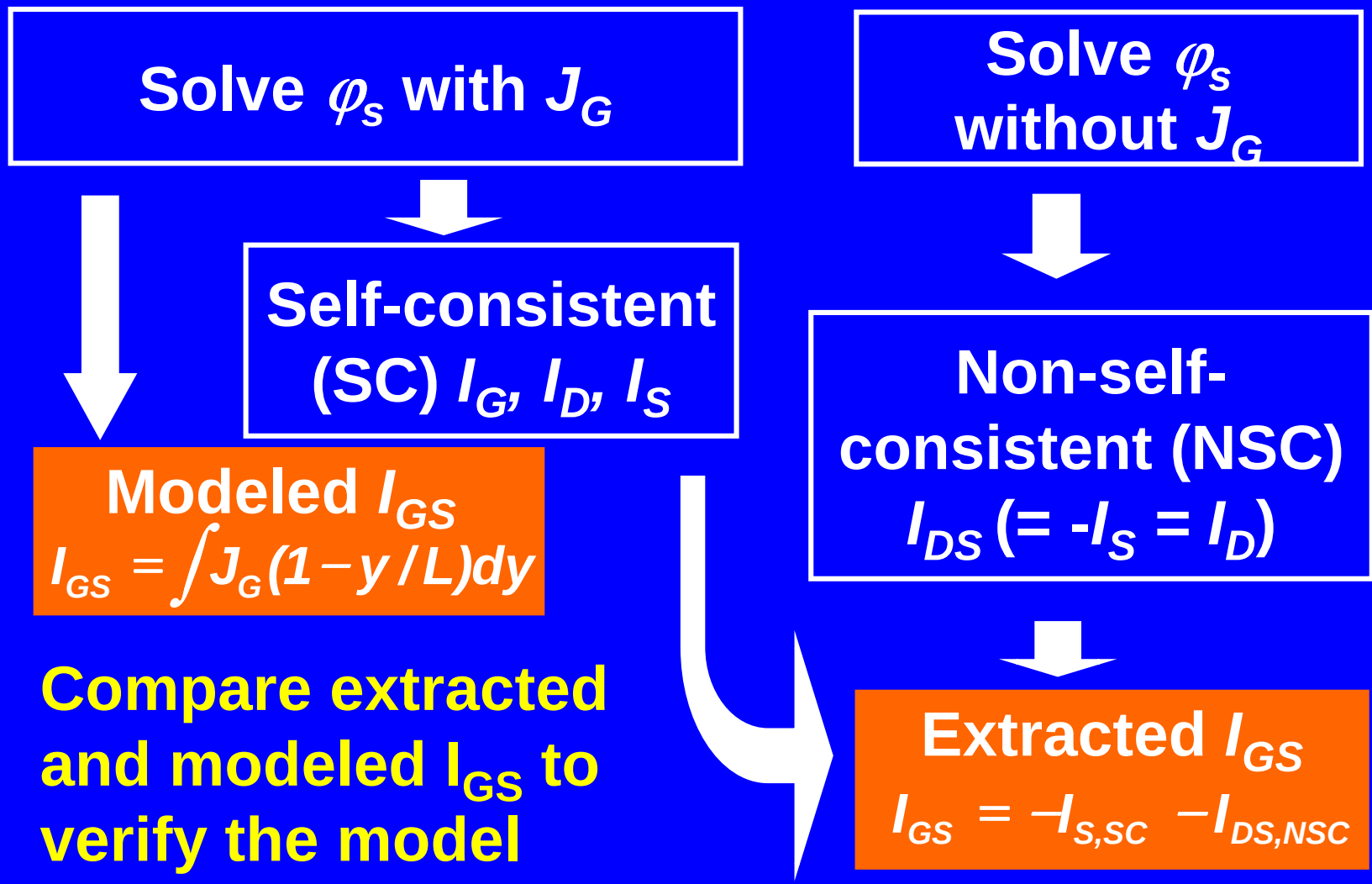
- **Parameters for the 130nm process technology* are used for validation.**
- **J_G parameters first calibrated to experimental data then set to ~ 1 kA / cm^2 at V_G =1.2 V (much higher than worst-case condition under BI).**

*S. Tyagi, *et al.*, IEDM Tech. Dig., p. 567, 2000.

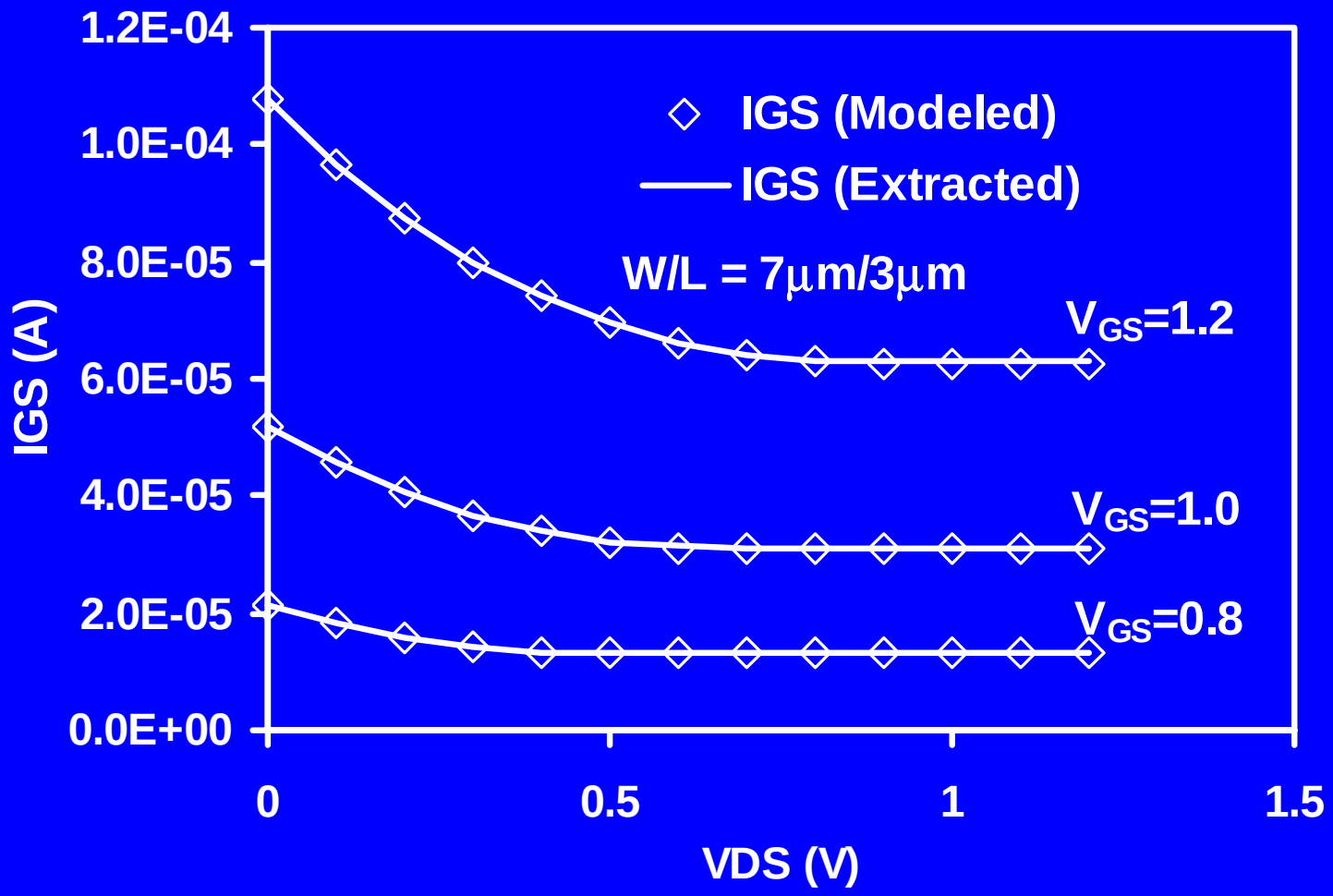
Hybrid Model vs. Exp.



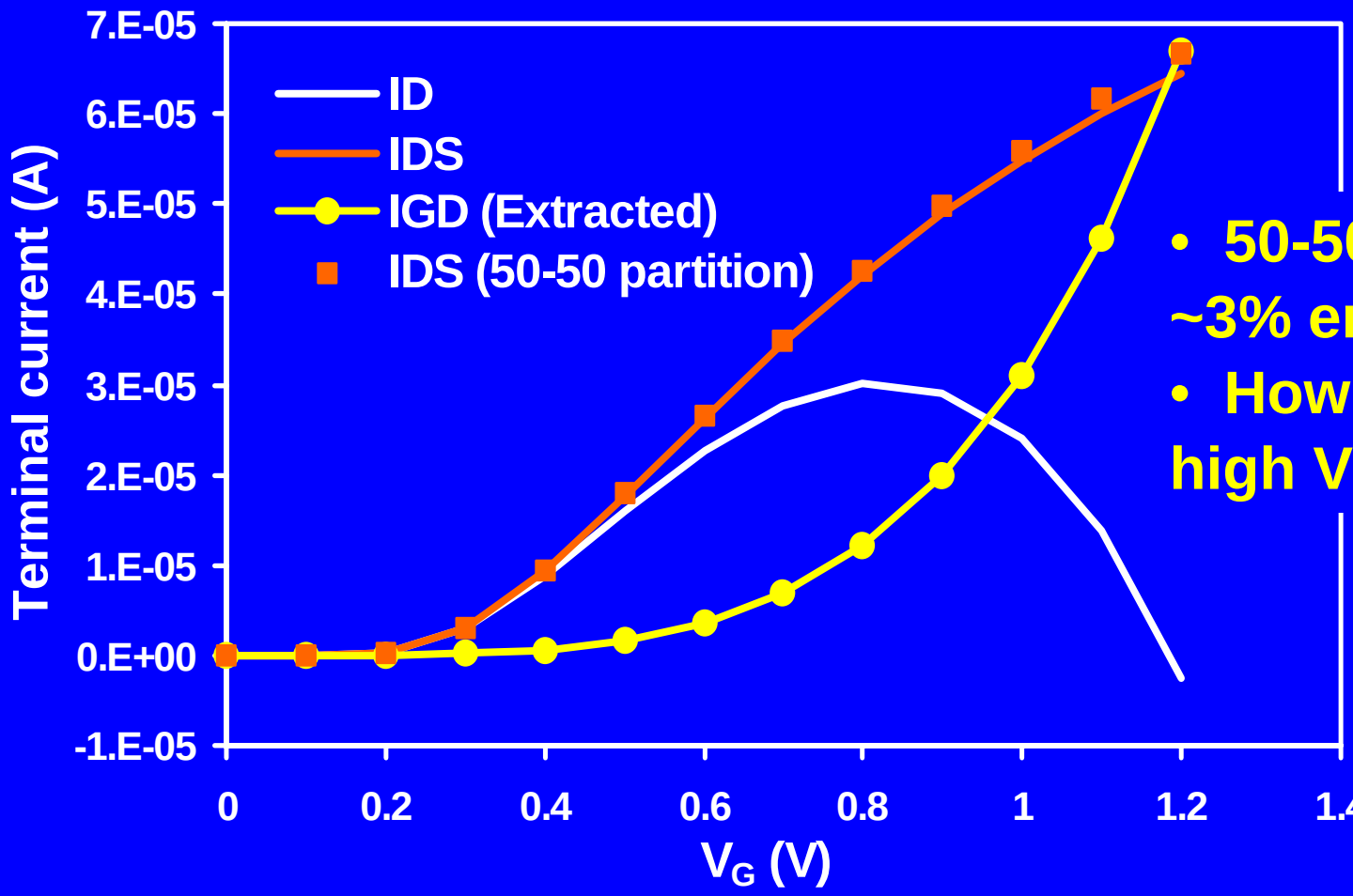
Validation Flow



Extracted vs. Modeled I_{GS} (Long Device, No Channel De-biasing)

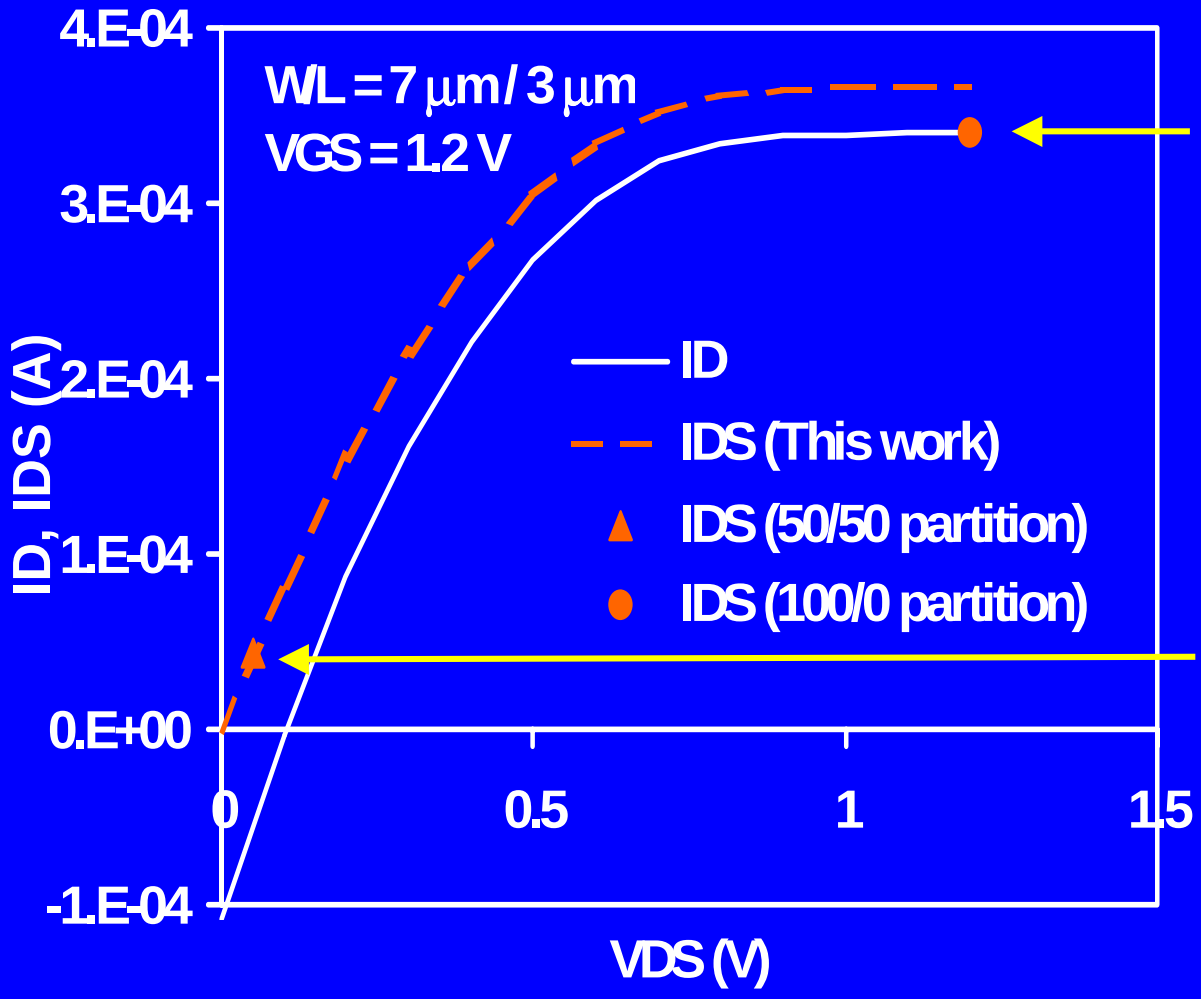


I_G Correction Needed for I_{DS} Extraction



- 50-50 partition ~3% error
- How about high V_{DS}?

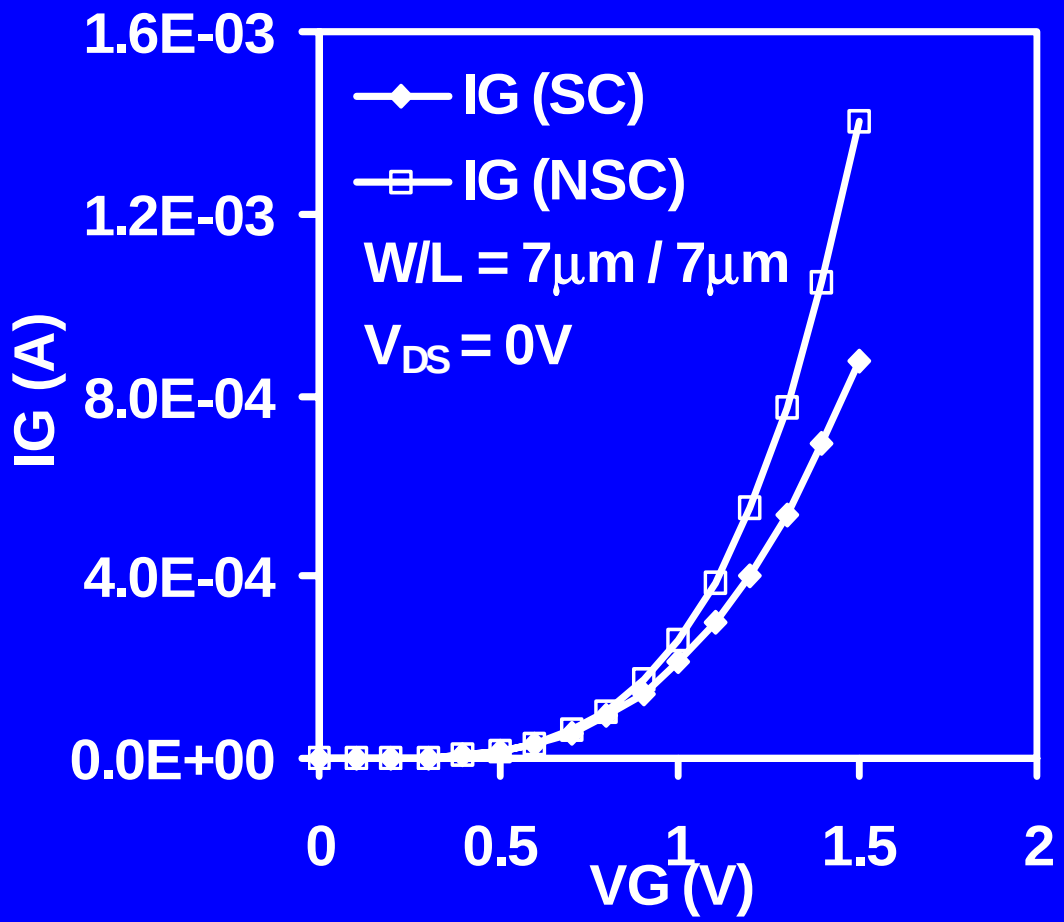
More Accurate I_{DS} Extraction



100-0 partition underestimates by ~ 10%

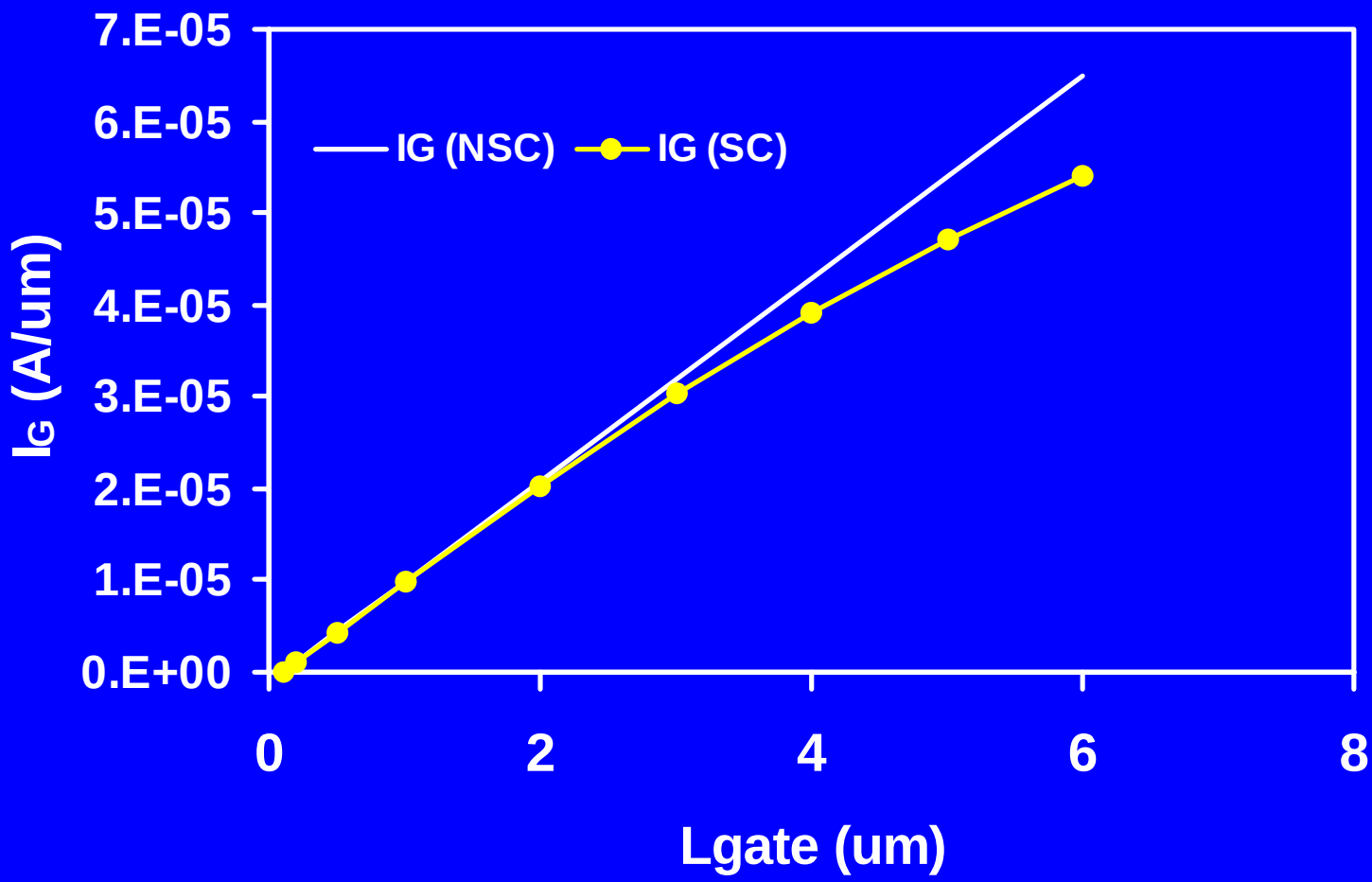
50-0 partition overestimates by ~ 5%

Channel De-Biasing Effects in Long Devices

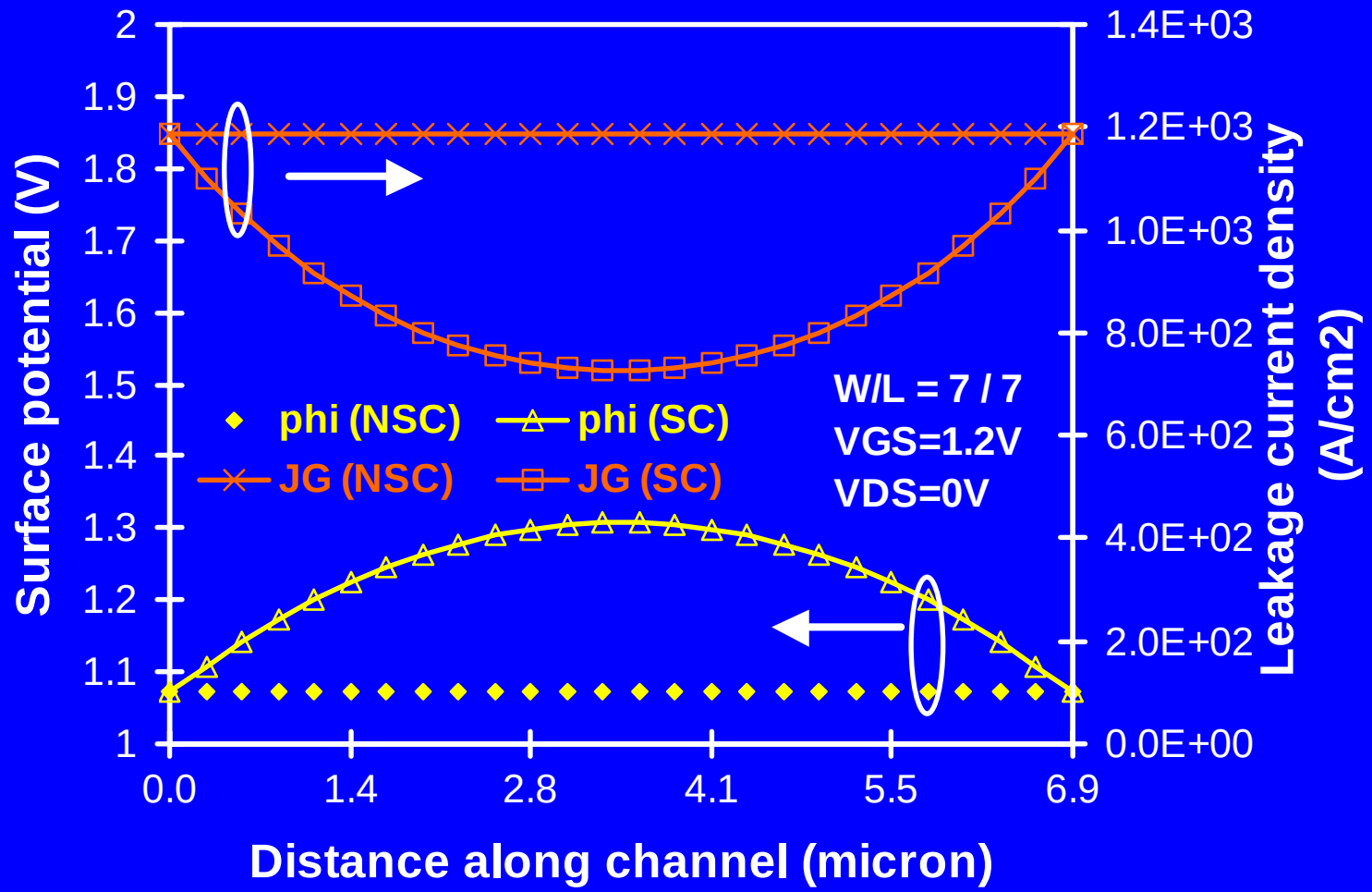


- Large difference between self-consistent and non-self-consistent I_G observed for L > 6 μm.
- IR drop across the resistive channel causes mid-channel φ_s to become higher than φ_{ss} and φ_{sd}

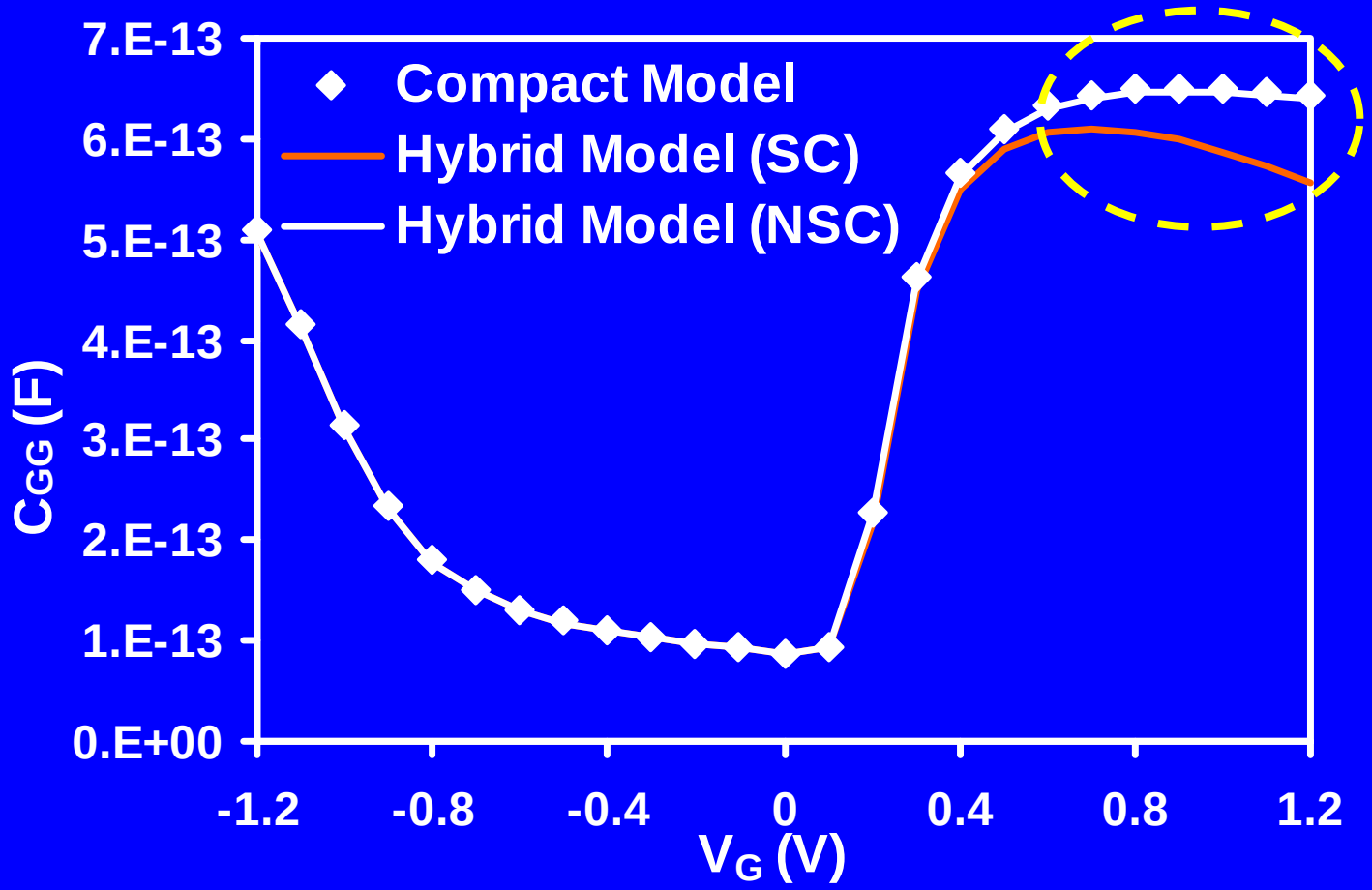
I_G Does Not Scale with L for Long Devices



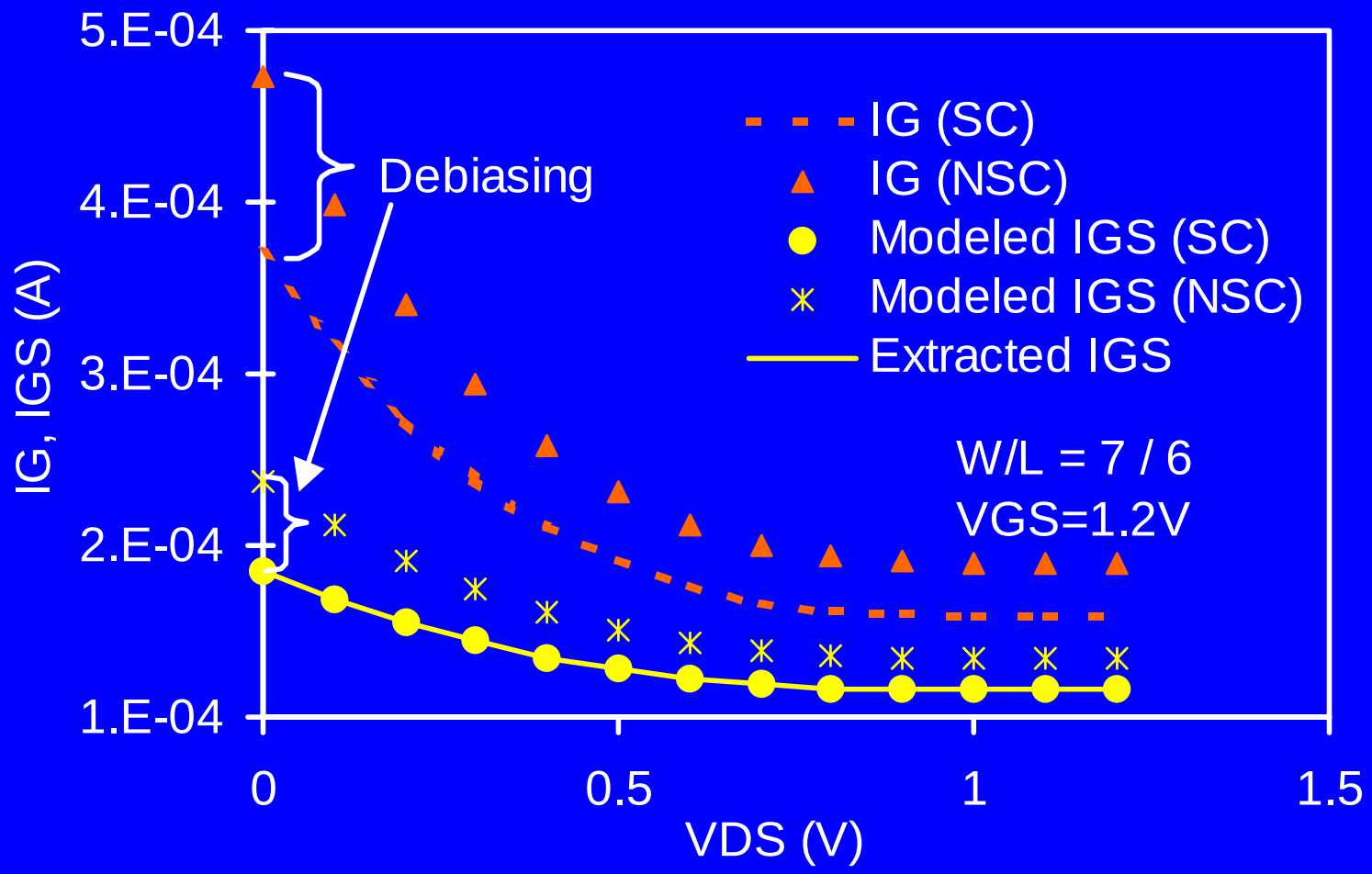
Channel De-Biasing Effects on Surface Potential & J_G



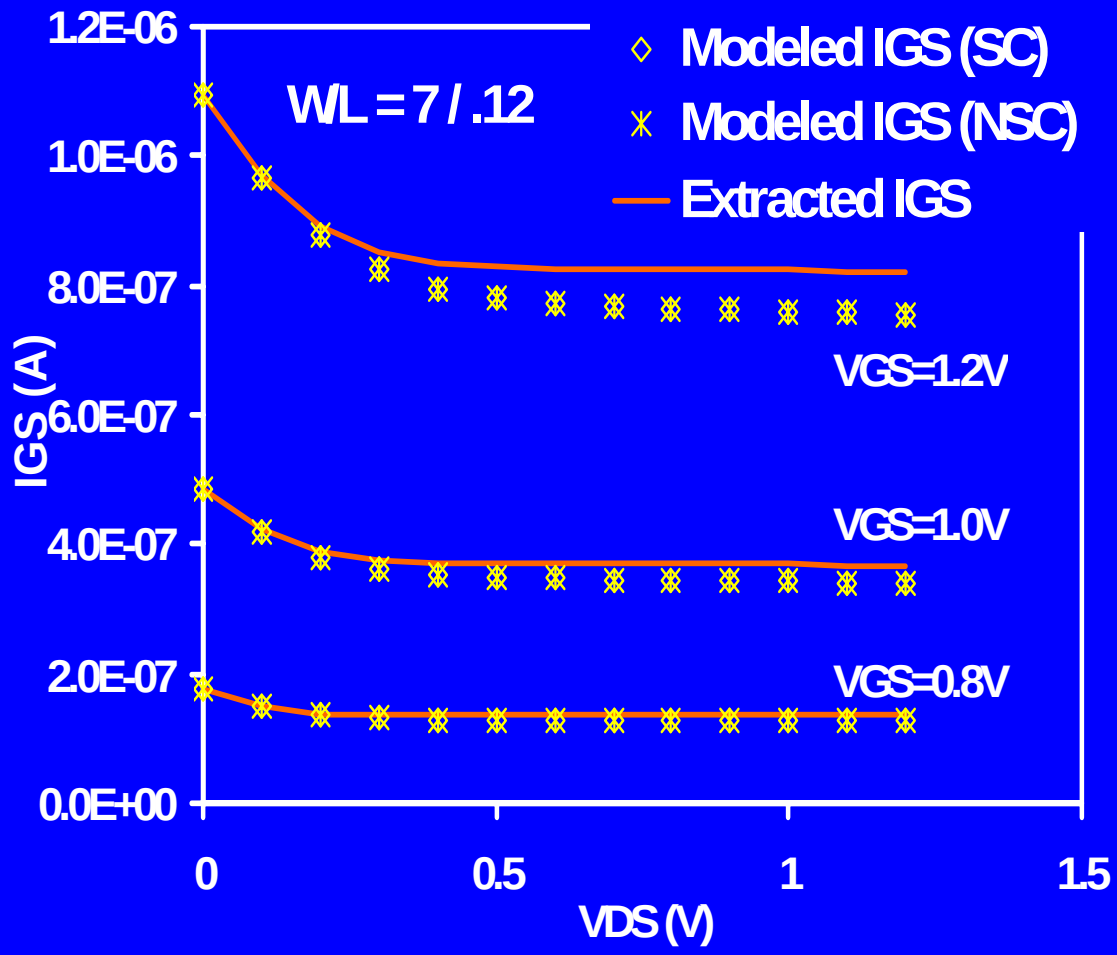
Channel De-Biasing Effect on Long-Channel C_{GG}



Partition Scheme Remains Valid with Channel De-Biasing

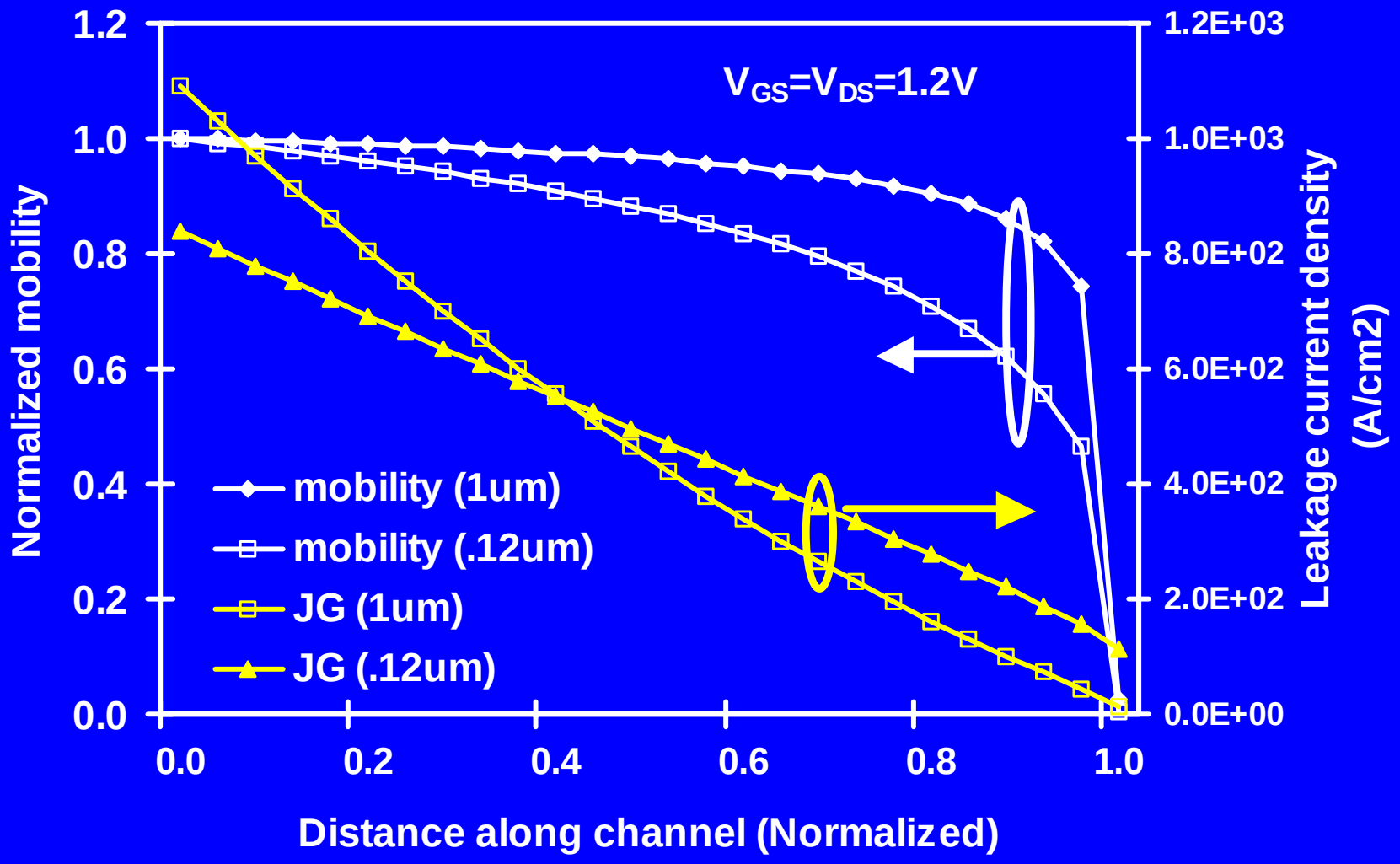


Extracted vs. Modeled I_{GS} (Short Device)



- Error due to constant-mobility assumption most significant in short devices. (~ 10%)
- Impact on I_D and I_S is insignificant since $I_{DS} >> I_G$

Cause of I_{GS} Underestimation



Summary

- A general I_G source/drain partition scheme is shown to be same as charge partition.
- Valid beyond weak tunneling regime, a critical assumption made in previous works.
- No detailed model formulation for the leakage density was assumed.

Summary

- A hybrid model developed for validation.
- In long devices where correct I_G partition is important, the partition scheme is accurate to within 1%.
- In short devices, ~ 10% error due to velocity saturation. Negligible impact on I_D.
- Considerable impact observed on extraction of long-channel saturation I_{DS}.

Acknowledgement

We thank Intel TCAD and PTD staff for encouragement and support on this project.